Amendments to the Specification:

Please amend the paragraph beginning at line 8 of page 5 and ending at line 9 of page 5 as follows:

Figure 2 provides a top view of an nMOSFET design layout for power ESD protection which is in accordance with an embodiment of the present invention;

Please amend the paragraph beginning at line 18 of page 5 and ending at line 20 of page 5 as follows:

Figures 7-10 are similar to Figures 2, 3, 4 and 6, but relate to an nMOSFET design layout for I/O ESD protection which is in accordance with another embodiment of the present invention.

Please amend the paragraph beginning at line 8 of page 6 and ending at line 20 of page 6 as follows:

Figs. 2 and 3 provide a top-view and a cross-sectional view, respectively, of an nMOSFET design layout which is in accordance with an embodiment of the present invention. A P-well 30 is underneath NMOS fingers 32 and is formed on a P-conductivity type substrate 34. The P-well 30 is surrounded by an N-well ring (VDD) 36. A lightly-doped P-type region ~~38~~ 34 having an impurity concentration lower than that of the P-well 30 is provided as underlying a field oxide film. The N-well ring 36 is designed so that the inner P-well 30 underneath the NMOS fingers 32 is separated from the outer P-well 40. The inner P-well 30 and outer P-well 40 are connected by a P-substrate resistance 42 which is much higher than the resistance of the P-

wells 30, 40. A P+-diffusion ring 44 surrounding the N-well ring 36 is configured to connect to VSS, i.e., P-taps. In Fig. 3, reference numerals 46 identify VSSIO interconnects, and reference numerals 48 identify VDD interconnects.

Please amend the paragraph beginning at line 1 of page 7 and ending at line 19 of page 7 as follows:

A schematic circuit diagram of one of the NMOS fingers 32 is shown in Fig. 4. As shown, a high-value N-well resistor 50 is disposed between the gates 52 and VSS ~~54~~ 46. Reference numeral 30 in Fig. 4 identifies the P-well which is underneath the NMOS fingers 32, reference numeral 40 identifies the outer P-well, reference numeral 42 identifies the substrate resistance and reference numeral 56 identifies a ~~dnw~~ N-well diode. In the positive ESD zapping, VDD pad voltage is increased. The gate nodes act as a high-pass filter because of drain-to-gate capacitance and the external N-well resistance, and thus will be coupled. After the gate is coupled, the substrate current of the NMOS fingers 32 increases. Fig. 5 shows the normalized DC substrate current in 0.13 μm node technology. In Fig. 5, gate voltage is provided along the horizontal axis, and the normalized substrate current is provided along the vertical axis (Lg = 0.24 μm, VDS = 2 volts). Since the NMOS P-well 30 is separated by the N-well ring 36, the substrate current flows into the high-resistance P-substrate 34. Furthermore, because the N-well ring 36 is connected to VDD, it suppresses (as identified by line 58 and arcs 60 in Fig. 6) the substrate current flowing to the VSS P-taps (i.e., the outer P-well 40) due to extension of P-

substrate depletion, i.e., increasing the effective substrate resistance 42. Thus, the NMOS P-well voltage is built-up, and triggers the parasitic bipolar transistors 62 (see Fig. 3) at low voltage.

Please amend the paragraph beginning at line 18 of page 10 and ending at line 22 of page 10 as follows:

In the negative ESD zapping, since the N-well is deeper than STI (Shallow-Trench Isolation), the ESD current can flow from P-taps (i.e., VSSIO) to I/O pad using the ~~P-Well/N-Well~~ P-well/N-well junction diode. Therefore, the N-Well ring 76 also provides a negative ESD path to avoid the ESD current flowing through the high-resistance P-substrate region 34.